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Fabrication of Photonic Crystal Structures by Focused Ion Beam Etching

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ABSTRACT

Two methods for Focused Ion Beam (FIB) etching of Photonic Crystal are presented. The first is a FIB-alone approach which is a very rapid, maskless process. This method has the disadvantage that it produces poor sidewall verticality, which leads to high losses in slab waveguide based systems. A second approach uses FIB to etch a metal mask layer, this is followed by RIE of a SiO_2 layer and a final ICP etch of the InP layer. Results show much improved sidewall verticality.

1. INTRODUCTION

Photonic crystals (PCs) are currently of considerable interest in applications as wide ranging as sensors to telecommunications. They are now being manufactured in large volumes by a number of research groups and companies around the world [1]. The techniques used in this manufacture have, thus far, been confined to either optical or e-beam lithography and some form of dry etching, in particular Reactive Ion Etching (RIE), Chemically Assisted Ion Beam Etching (CAIBE) and Inductively Coupled Plasma (ICP) etching [2]. This usually involves lengthy exposure times and at least one mask transfer process. Focused Ion Beam (FIB) etching however, enables "direct write" photonic crystals to be formed with design of mask to manufactured device of 2 hours or less. The FIB etching process involves directing a beam of highly focused Ga^+ ions at a sample surface under computer control. The surface is then ablated by the Ga^+ ions leaving a relief pattern. This ability is almost material independent, with only the etch rate and profiles changing with material. It is this speed and flexibility that makes this process particularly attractive. Unfortunately, there are disadvantages to this approach in particular, due the nature of FIB etching, it is very difficult to obtain good side wall verticality in holes and as will be discussed below, this leads to increased losses [3]. In order to overcome this problem a multistage approach is being adopted whereby FIB is used to define a top metal mask layer and then more traditional RIE and ICP etch steps are used to transfer the mask into a slab waveguide structure. Although this reduces the speed and flexibility of the approach, it is still felt that the high resolution obtainable with FIB etching and the lack of problems such as proximity effects could make FIB based PC fabrication a viable alternative to E-beam based methods. This paper presents results for fabrication and measurement of FIB-alone based PCs and then shows preliminary fabrication results for a multistage FIB based method.

2. RESULTS

2.1 FIB-Alone Method

If a series of points are defined at regular intervals it is possible to form a photonic crystal structure by focused ion beam etching a typical structure is shown in Fig 1. The photonic Crystal has been etched into a 3 layer slab guide structure such that light can be guided through the PC region in order to perform transmission tests on the device.



Figure 1. Photonic crystal fabricated by a FIB.

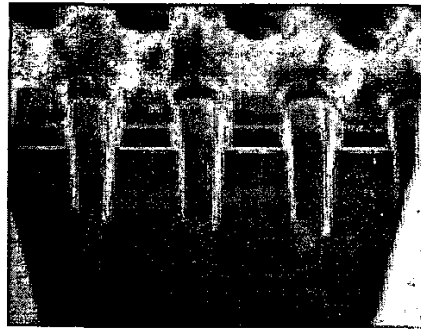


Figure 2. Detail of holes etched FIB-Alone method.

Extensive studies have been carried out into this process on InP, showing that excess etch [4] and side wall verticality may be a limiting factor. Inset in Fig. 1 and Fig. 2 show cross sections through typical holes in InP, showing a sidewall angle of approximately 6° .

For the structure in Fig. 1 a lattice constant of 375nm and a design r/a of 0.3 was used. The PC region covered an area of $38\text{ }\mu\text{m}$ by 16 rows. The r/a at the guiding layer is considerably less than 0.3 at around 0.24 due to the side wall angle. Etching took place with a beam current of 150 pA to a depth of approximately $1\text{ }\mu\text{m}$. The structure was etched in a slab guide such that the transmission response could be measured. The lattice constant was chosen such that there would be a band edge in the region of 1480 nm to 1640 nm, the range available for transmission tests. Figure 3 shows the results for these tests alongside modelled results obtained from Translight [5].

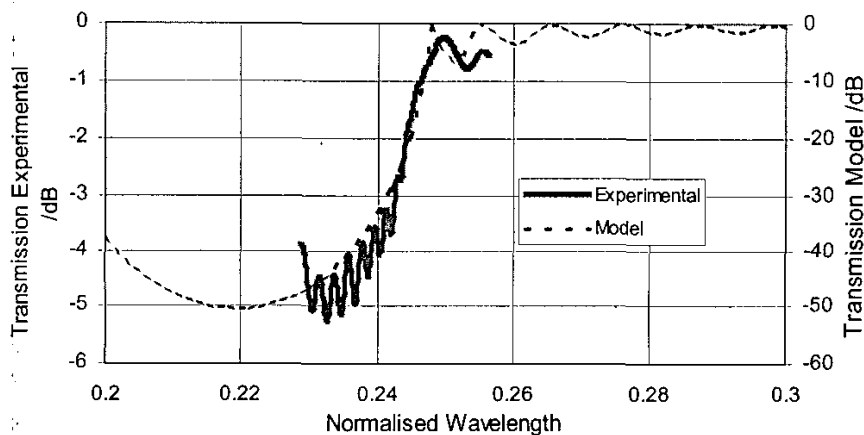


Fig 3. Measured and modelled transmission results.

The modelled results used a background $\epsilon_r = 10.24$ and an r/a value of 0.24. There is a clear agreement with band edge position, however the depth of the transmission minimum is many times less than predicted. Finite Difference Time Domain modelling of photonic crystals with tapered holes [3] has shown both a reduction in the transmission minimum and a reduction in the band edge roll off. It is therefore suggested that in low vertical contrast waveguide structures FIB etching is not ideally suited to photonic crystal manufacture. The next section outlines a multistage process that should enable much improved performance to be obtained.

2.2 Multistage FIB-Based Method

It is also possible to use FIB etching in the same way that e-beam lithography is used. Doing this removes a masking step, as it is no longer necessary to use a polymer for the first exposed mask. In this method mask layers of SiO_2 and Nickel are deposited on top of the InP wafer. Firstly, the metal mask is directly etched with the desired pattern. This is then transferred to the SiO_2 layer by RIE. This is followed by an ICP etch of the InP in order to produce deep vertical holes. Results for the first stage SiO_2 etching are shown in Fig. 4. The excellent

sidewall verticality in the SiO_2 mask is seen, as is the quality of the holes in the metal mask. This image has been formed by cross sectioning also using the FIB etching machine.

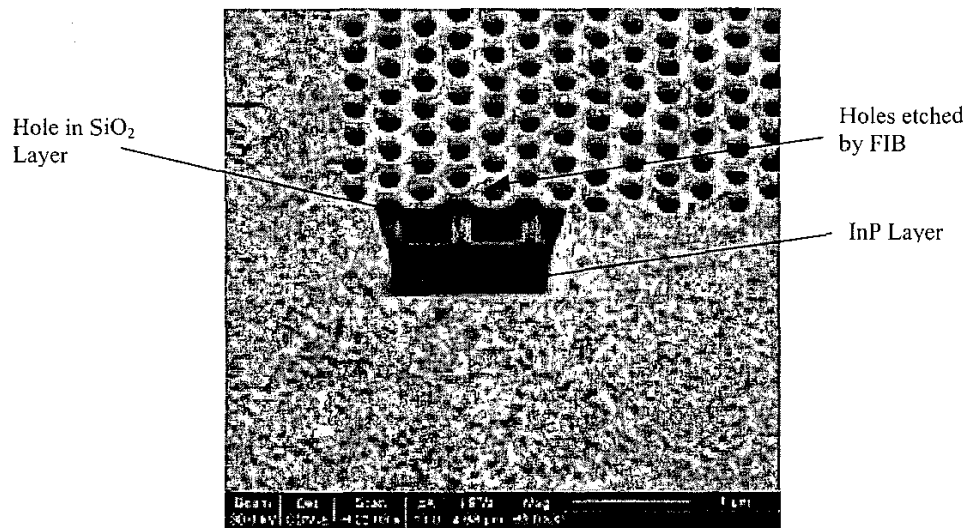


Figure 4. FIB etched metal mask with RIE etched SiO_2 layer.

This stage is then followed by ICP etching of the InP layer, figure 5 shows results for this stage. Here the ability of the FIB to deposit metal, in this case Platinum has been used to fill the etched holes in order to make cross sectioning with the FIB more accurate.

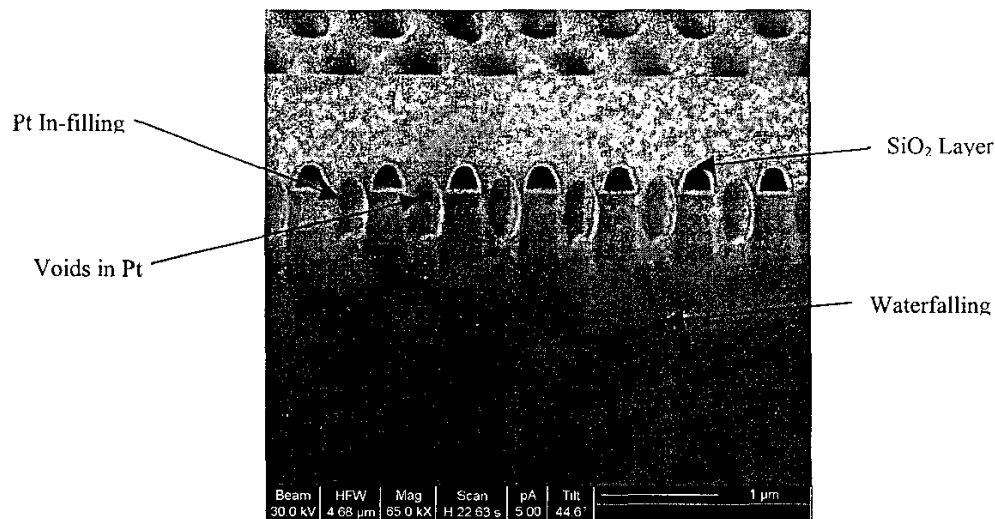


Fig 5. Final stage of ICP etching of InP layer with Pt in-filling of holes.

It can be seen that improved verticality has now been obtained and with further optimisation of the ICP etch stage deep vertical side walls holes should be obtainable.

3. CONCLUSIONS

This paper has presented results for two FIB based methods for fabricating PC based devices. In the first method FIB-Alone processing is used, this is a very rapid and flexible maskless process. However, it results in poor sidewall verticality which leads to increased losses in slab guide PC devices. This approach may be more suited to membrane and SOI technologies which suffer less from out-of-plane scattering. A second approach whereby FIB is used to etch a metal mask, followed by RIE etching of a SiO_2 layer and a final ICP etch of the InP layer

has also been shown. The results for this are very encouraging and work is on-going to optimise the ICP stage to produce deep vertical holes, required for high performance PC devices in InP slab waveguide systems.

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